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DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>28 July 2004</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-23</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-23</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>29 December 2000</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date <u>7/28/04</u>.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

## DETAILED ACTION

1.      Claims 1-23 have been examined.

### *Papers Received*

·2.      Receipt is acknowledged of information disclosure statement and amendment

papers submitted, where the papers have been placed of record in the file.

3.      The amendment has overcome the some of the objections to the claims and the

objections to the specification and drawings, which are herein withdrawn. The Examiner

notes that one of the claim objections remains as given below.

### *Claim Objections*

4.      Claim 22 objected to because of the following informalities:  lines 3-4 states,

"plurality coprocessors" when it should read "plurality of coprocessors".

### *Claim Rejections - 35 USC § 103*

5.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.      Claims 1-8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Moyer (5,983,338) in view of Strongin (6,559,850 B1).

7.      In regard to claim 1,

      a.      Moyer has disclosed an interface (figure 1, element 30) for transferring

      data between a central processing unit (CPU) (figure 1, element 12) and a

      plurality of coprocessors (figure 1, elements 14 and 16), the interface comprising:

      i.     an instruction bus (column 6, line 34 and figures 2 and 3, element 61), configured to transfer instructions to the plurality of coprocessors in an instruction transfer order (an order is inherent), wherein particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU (figures 22-26, UU field); and

      ii.    a data bus (column 8, lines 65-66 and figures 2 and 3, element 72), coupled to said instruction bus (since both go from processor to coprocessor, they are coupled), configured to subsequently transfer the data.

b.     Moyer does not disclose wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

c.     Strongin has disclosed in figures 3 and 4 a read retrieval order that differs from the read request order. An instruction as in Moyer is essentially a request for data or a read request. When the data is sent, that is a read retrieval. The figure shows signals (identifier) that indicate the order of the data.

d.     Strongin has shown in column 6, lines 36-44 that this difference in ordering allows for data accesses to be quicker. This quickness of data access would have motivated one of ordinary skill in the art to modify the design of Moyer to include the out of order data retrieval disclosed by Strongin. With this

modification in place, the data order signals would prescribe transfer of a data

element corresponding to a specific outstanding instruction relative to all

outstanding instructions. Since the disclosure of Moyer is dealing with the

transfer of data between a processor and coprocessors, the data is inherently

associated with outstanding instructions and further it is inherent that the

instruction is relative to all other instructions in some manner. This relation could

simply be instruction order, which would then mean that the outstanding

instruction is relative to the other instructions in that some are before it and some

after in program order.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the design of Moyer to retrieve data out of order as taught by Strongin so that

data accesses can be achieved quicker.

8.      In regard to claim 2,

a.      Moyer in view of Strongin discloses the interface as recited in claim 1, as

described above;

b.      Moyer in view of Strongin does not disclose specifically that the plurality of

coprocessors comprises: a first plurality of floating-point coprocessors;

c.      Moyer has shown in column 1, lines 31-37 that a traditional use of

coprocessors is as floating-point coprocessors.

d.      The ability to extend the functionality of the processor disclosed by Moyer

by including floating point processing would have motivated one of ordinary skill

in the art to modify the coprocessor design of Moyer in view of Strongin to making them floating-point processors.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer in view of Strongin to make the disclosed coprocessors floating-point coprocessors in order to extend the functionality of the main processor.

9.    In regard to claim 3, Moyer in view of Strongin discloses the interface as recited in claim 1, as described above, wherein said particular instructions comprise TO instructions, said TO instructions directing that the subsequent transfer of the data will be from the CPU to said designated ones of the plurality of coprocessors. Column 9, lines 27-28 of Moyer, show an H_CALL instruction that transfers data from an external coprocessor to the processor as shown in lines 40-45.

10.    In regard to claim 4, Moyer in view of Strongin discloses the interface as recited in claim 3, as described above, wherein said particular instructions comprise FROM instructions, said FROM instructions directing that the subsequent transfer of the data will be from the CPU to said designated ones of the plurality of coprocessors. [Column 9, lines 27-39 of Moyer, show an H_CALL instruction that transfers data to an external coprocessor from the processor.]

11.    In regard to claim 5, Moyer in view of Strongin discloses the interface as recited in claim 4, as described above, wherein said data bus comprises:

a.    data TO signals, for transferring data from the CPU to said designated ones of the plurality of coprocessors (Moyer, column 9, lines 20-25);

      b.     data FROM signals, for transferring data to the CPU from said designated

ones of the plurality of coprocessors (Moyer, column 9, lines 25-27).

12.    In regard to claim 6, Moyer in view of Strongin discloses the interface as recited

in claim 5, as described above, wherein said data order signals comprise:

      a.     TO order signals, for prescribing said data transfer order with respect to

transfers via said data TO signals; and

      b.     FROM order signals, for prescribing said data transfer order with respect

to transfers via said data FROM signals.

[Since the order signals prescribe data order for all data accesses the data order is

prescribed for data going to and from the coprocessors.  Thus the signals can be called

TO and FROM order signals respective to the coprocessors.]

13.    In regard to claim 7, Moyer in view of Strongin discloses the interface as recited

in claim 6, as described above, wherein said TO order signals prescribe a particular

outstanding TO instruction relative to all outstanding TO instructions.  [Figure 4 and

column 10, lines 46-61 of Strongin, show that the order signals (identifiers) give

indication of which instruction (read request) the data corresponds to.  This instruction is

relative to the other outstanding (pending) instructions.  For example instruction (read

request) 100N follows instruction 100I and is thus relative to it.]

14.    In regard to claim 8, Moyer in view of Strongin discloses the interface as recited

in claim 6, as described above, wherein said FROM order signals prescribe a particular

outstanding FROM instruction relative to all outstanding FROM instructions.  [Figure 4

and column 10, lines 46-61 of Strongin, show that the order signals (identifiers) give

indication of which instruction (read request) the data corresponds to. This instruction is

relative to the other outstanding (pending) instructions. For example instruction (read

request) 100N follows instruction 1001 and is thus relative to it.]

15.     In regard to claim 22,

         a.     Moyer has disclosed a method for transferring data (via figure 1, element

30) between a CPU (figure 1, element 12) and a plurality of coprocessors (figure

1, elements 14 and 16), the method comprising:

                 i.      transmitting instructions to the plurality coprocessors (column 6,

         lines 34-36), each of the instructions directing a data transfer between the

         CPU and a specific coprocessor (figures 22-26, UU field), wherein said

         transmitting is provided in a specific instruction order (an order is

         inherent);

         b.     Moyer does not disclose transferring the data in an order different from the

specific instruction order, prescribing transfer of a data element corresponding to

a specific outstanding instruction relative to all outstanding instructions, the

outstanding instructions being those instructions that have not completed a

subsequent data transfer.

         c.     Strongin has disclosed in figures 3 and 4 a read retrieval order that differs

from the read request order. An instruction as in Moyer is essentially a request

for data or a read request. When the data is sent, that is a read retrieval. The

figure shows signals (identifier) that indicate the order of the data. Figure 4 and

column 10, lines 46-61 of Strongin, show that the order signals (identifiers) give

indication of which instruction (read request) the data corresponds to. This

instruction is relative to the other outstanding (pending) instructions. For

example instruction (read request) 100N follows instruction 100I and is thus

relative to it.

d.      Strongin has shown in column 6, lines 36-44 that this difference in

ordering allows for data accesses to be quicker. This quickness of data access

would have motivated one of ordinary skill in the art to modify the design of

Moyer to include the out of order data retrieval disclosed by Strongin.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the design of Moyer to retrieve data out of order as taught by Strongin so that

data accesses can be achieved quicker.

16.    Claims 9 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Moyer in view of Strongin as applied to claims 1-8 and 22 above, and further in view of

Hennessy.

17.    In regard to claim 9,

a.      Moyer in view of Strongin discloses the interface as recited in claim 1, as

described above,

b.      Moyer in view of Strongin does not disclose wherein said data bus

transfers the data in parallel to one of said designated ones of the plurality of

coprocessors, said one of said designated ones of the plurality of coprocessors

having multiple issue pipelines providing for parallel instruction execution.

c.      Hennessy has shown on pages 282-284 a multiple instruction issue

technique.  This inherently involves multiple data elements and thus the data bus

to such a processor transfers data in parallel.

`      d.      Hennessy has shown on page 278 that multiple-issue processors allow

multiple instructions to issue each clock cycle.  It is further shown that this

decreases CPI below one and increases performance.  This performance boost

would have motivated one of ordinary skill in the art to modify the design of

Moyer in view of Strongin to use the multiple issue technique described by

Hennessy for its coprocessors.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the coprocessors and data bus of Moyer in view of Strongin to include the

multiple instruction issue technique taught by Moyer in view of Strongin in order to

increase performance of the overall system.

18.      In regard to claim 23,

a.      Moyer in view of Strongin discloses the method as recited in claim 22, as

described above, said transmitting comprises:

b.      Moyer in view of Strongin does not disclose

i.      issuing a plurality of the instructions in parallel to the specific

coprocessor;

ii.      designating an execution order corresponding to said issuing.

c.      Hennessy has shown on pages 282-284 a multiple instruction issue

technique.  This inherently involves multiple instructions and thus the bus to such

a processor transfers instructions in parallel.

d.      Hennessy has shown on page 278 that multiple-issue processors allow

multiple instructions to issue each clock cycle.  It is further shown that this

decreases CPI below one and increases performance.  This performance boost

would have motivated one of ordinary skill in the art to modify the design of

Moyer in view of Strongin to use the multiple issue technique described by

Hennessy for its coprocessors.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the coprocessors and data bus of Moyer in view of Strongin to include the

multiple instruction issue technique taught by Moyer in view of Strongin in order to

increase performance of the overall system.

19.     Claims 10-12 and 14-20 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Moyer in view of Tanenbaum and further in view of Strongin.

20.     In regard to claim 10,

a.      Moyer discloses a computer program product for use with a computing

device, the computer program product comprising:

i.      a computer usable medium,  for causing a coprocessor interface to

be described that transfers data between CPU and a plurality of

coprocessors, said computer readable program code comprising:

(1)     an instruction bus, said instruction bus configured to transfer

instructions to said plurality of coprocessors in an instruction

transfer order, wherein particular instructions direct designated

ones of the plurality of coprocessors to transfer said data to/from

said CPU; and

(2)     a data bus, said data bus configured to subsequently

transfer said data.

b.      Moyer does not disclose having computer readable program code

embodied in said medium and first program code and second program code.

Moyer also does not disclose wherein data order signals within said data bus

prescribe a data transfer order that differs from said instruction transfer order and

wherein said data order signals prescribe transfer of a data element

corresponding to a specific outstanding instruction relative to all outstanding

instructions.

c.      Tanenbaum has disclosed on pages 10-12 that hardware is logically

equivalent to software and that the boundaries between them are fluid.  Strongin

has disclosed in figures 3 and 4 a read retrieval order that differs from the read

request order.  An instruction as in Moyer is essentially a request for data or a

read request.  When the data is sent, that is a read retrieval.  The figure shows

signals (identifier) that indicate the order of the data.

d.      Tanenbaum has shown on page 11 that for one factor involved in deciding

whether to implement a function in hardware or software is frequency of change.

It is easier to change software code than to change the layout of a hardware system. This ease of change would have motivated one of ordinary skill in the art to modify the design of Moyer to implement the disclosed apparatus as program code as taught by Tanenbaum. Strongin has shown in column 6, lines 36-44 that this difference in ordering allows for data accesses to be quicker. This quickness of data access would have motivated one of ordinary skill in the art to modify the design of Moyer to include the out of order data retrieval disclosed by Strongin. With this modification in place, the data order signals would prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions. Since the disclosure of Moyer is dealing with the transfer of data between a processor and coprocessors, the data is inherently associated with outstanding instructions and further it is inherent that the instruction is relative to all other instructions in some manner. This relation could simply be instruction order, which would then mean that the outstanding instruction is relative to the other instructions in that some are before it and some after in program order.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to implement his design in program code as taught by Tanenbaum and to retrieve data out of order as taught by Strongin so that data accesses can be achieved quicker and so that changes may be made easier.

21.     In regard to claim 11, Moyer in view of Tanenbaum and further in view of

Strongin discloses the computer program product as recited in claim 10, as described

above, wherein said particular instructions comprise:

> a.      TO instructions, said TO instructions directing that the subsequent transfer
>
> of said data will be from said CPU to said designated ones of said plurality of
>
> coprocessors; [Column 9, lines 27-28 of Moyer, show an H_CALL instruction that
>
> transfers data from an external coprocessor to the processor as shown in lines
>
> 40-45.]
>
> b.      FROM instructions, said FROM instructions directing that the subsequent
>
> transfer of said data will be to said CPU from said designated ones of said
>
> plurality of coprocessors.  [Column 9, lines 27-39 of Moyer, show an H_CALL
>
> instruction that transfers data to an external coprocessor from the processor.]

22.     In regard to claim 12, Moyer in view of Tanenbaum and further in view of

Strongin discloses the computer program product: as recited in claim 11, as described

above, wherein said data order signals comprise:

> a.      TO order signals, for specifying said data transfer order for a particular
>
> outstanding TO instruction relative to all outstanding TO instructions;
>
> b.      FROM order signals, for specifying said data transfer order for a particular
>
> outstanding FROM instruction relative to all outstanding FROM instructions.

[Since the order signals prescribe data order for all data accesses the data order is

prescribed for data going to and from the coprocessors.  Thus the signals can be called

TO and FROM order signals respective to the coprocessors.]

23.    In regard to claim 14,

    a.    Moyer discloses a computer data signal embodied in a transmission medium, the computer data signal comprising:

        i.    an instruction bus, said instruction bus configured to transfer instructions to said plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer said data to/from said CPU; and

        ii.    a data bus, said data bus configured to subsequently transfer said data.

    b.    Moyer does not disclose having computer-readable program code for providing the above. Moyer also does not disclose wherein data order signals within said data bus prescribe a data-transfer order that differs from said instruction transfer order.

    c.    Tanenbaum has disclosed on pages 10-12 that hardware is logically equivalent to software and that the boundaries between them are fluid. Strongin has disclosed in figures 3 and 4 a read retrieval order that differs from the read request order. An instruction as in Moyer is essentially a request for data or a read request. When the data is sent, that is a read retrieval. The figure shows signals (identifier) that indicate the order of the data.

    d.    Tanenbaum has shown on page 11 that for one factor involved in deciding whether to implement a function in hardware or software is frequency of change. It is easier to change software code than to change the layout of a hardware

system. This ease of change would have motivated one of ordinary skill in the

art to modify the design of Moyer to implement the disclosed apparatus as

program code as taught by Tanenbaum. Strongin has shown in column 6, lines

36-44 that this difference in ordering allows for data accesses to be quicker. This

quickness of data access would have motivated one of ordinary skill in the art to

modify the design of Moyer to include the out of order data retrieval disclosed by

Strongin.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the design of Moyer to implement his design in program code as taught by

Tanenbaum and to retrieve data out of order as taught by Strongin so that data

accesses can be achieved quicker and so that changes may be made easier.

24.     In regard to claim 15, Moyer in view of Tanenbaum and further in view of

Strongin discloses the computer data signal as recited in claim 14, as described above,

wherein said particular instructions comprise TO instructions, said TO instructions

directing that subsequent transfer of said data will be from said CPU to said particular

coprocessors. [Column 9, lines 27-28 of Moyer, show an H_CALL instruction that

transfers data from an external coprocessor to the processor as shown in lines 40-45.]

25.     In regard to claim 16, Moyer in view of Tanenbaum and further in view of

Strongin discloses the computer data signal as recited in claim 15, as described above,

wherein said particular instructions comprise TO instructions, said TO instructions

directing that subsequent transfer of said data will be from said CPU to said particular

coprocessors. [Column 9, lines 27-39 of Moyer, show an H_CALL instruction that transfers data to an external coprocessor from the processor.]

26.     In regard to claim 17, Moyer in view of Tanenbaum and further in view of Strongin discloses the computer data signal as recited in claim 14, wherein said data bus comprises:

      a.      data TO signals, for transferring data from said CPU to said particular coprocessors (Moyer, column 9, lines 20-25);; and

      b.      data FROM signals, for transferring data to said CPU from said particular coprocessors (Moyer, column 9, lines 25-27).

27.     In regard to claim 18, Moyer in view of Tanenbaum and further in view of Strongin discloses the computer data signal as recited in claim 17, wherein said data order signals comprise:

      a.      TO order signals, for prescribing said data transfer order with respect to transfers via said data TO signals; and

      b.      FROM order signals, for prescribing said data transfer order with respect to transfers via said data FROM  signals.

[Since the order signals prescribe data order for all data accesses the data order is prescribed for data going to and from the coprocessors.  Thus the signals can be called TO and FROM order signals respective to the coprocessors.]

28.     In regard to claim 19, Moyer in view of Tanenbaum and further in view of Strongin the computer data signal as recited in claim 18, wherein said TO order signals prescribe a particular outstanding TO instruction relative to all outstanding TO

instructions. [ Figure 4 and column 10, lines 46-61 of Strongin, show that the order

signals (identifiers) give indication of which instruction (read request) the data

corresponds to. This instruction is relative to the other outstanding (pending)

instructions. For example instruction (read request) 100N follows instruction 100I and

is thus relative to it.]

29.     In regard to claim 20, Moyer in view of Tanenbaum and further in view of

Strongin discloses the computer data signal as recited in claim 18, wherein said FROM

order signals prescribe a particular outstanding FROM instruction relative to all

outstanding FROM instructions. [Figure 4 and column 10, lines 46-61 of Strongin, show

that the order signals (identifiers) give indication of which instruction (read request) the

data corresponds to. This instruction is relative to the other outstanding (pending)

instructions. For example instruction (read request) 100N follows instruction 100I and

is thus relative to it.]

30.     Claims 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Moyer in view of Tanenbaum and further in view of Strongin as applied to claims

10-12 above, and further in view of Hennessy.

31.     In regard to claim 13,

     a.     Moyer in view of Tanenbaum and further in view of Strongin discloses the

     computer program product as recited in claim 10, as described above,

     b.     Moyer in view of Tanenbaum and further in view of Strongin does not

     disclose wherein said data bus is configured to transfer said data in parallel to

particular coprocessors that have multiple issue pipelines providing for parallel

instruction execution and corresponding data transfers.

c.      Hennessy has shown on pages 282-284 a multiple instruction issue

technique.  This inherently involves multiple data elements and thus the data bus

to such a processor transfers data in parallel.

d.      Hennessy has shown on page 278 that multiple-issue processors allow

multiple instructions to issue each clock cycle.  It is further shown that this

decreases CPI below one and increases performance.  This performance boost

would have motivated one of ordinary skill in the art to modify the design of

Moyer in view of Strongin to use the multiple issue technique described by

Hennessy for its coprocessors.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the coprocessors and data bus of Moyer in view of Strongin to include the

multiple instruction issue technique taught by Moyer in view of Strongin in order to

increase performance of the overall system.

32.    In regard to claim 21,

a.      Moyer in view of Tanenbaum and further in view of Strongin discloses the

computer program product as recited in claim 14, as described above,

b.      Moyer in view of Tanenbaum and further in view of Strongin does not

disclose wherein said data bus is configured to transfer said data in parallel to

particular coprocessors that have multiple issue pipelines providing for parallel

instruction execution and corresponding data transfers.

c.      Hennessy has shown on pages 282-284 a multiple instruction issue

technique.  This inherently involves multiple data elements and thus the data bus

to such a processor transfers data in parallel.

d.      Hennessy has shown on page 278 that multiple-issue processors allow

multiple instructions to issue each clock cycle.  It is further shown that this

decreases CPI below one and increases performance.  This performance boost

would have motivated one of ordinary skill in the art to modify the design of

Moyer in view of Strongin to use the multiple issue technique described by

Hennessy for its coprocessors.

It would have been obvious to one of ordinary skill in the art at the time of invention to

modify the coprocessors and data bus of Moyer in view of Strongin to include the

multiple instruction issue technique taught by Moyer in view of Strongin in order to

increase performance of the overall system.

### Response to Arguments

33.     Applicant's arguments filed 4/8/04 have been fully considered but they are not

persuasive.

34.     Applicant has argued throughout the remarks with respect to claims 1-23 that

neither Moyer nor Strongin provide teaching or motivation that would lead one skilled in

the art to provide for data order signals that prescribe transfer of a data element

corresponding to a specific outstanding instruction *relative to all other instructions*.  The

Examiner would like to point out that this new limitation that states, "and wherein said

data order signals prescribe transfer of a data element corresponding to a specific

outstanding instruction relative to all outstanding instructions," is very broad and in

actuality doesn't seem to further limit the claim language from the previous version of

the claims. Since the disclosure of Moyer is dealing with the transfer of data between a

processor and coprocessors, the data is inherently associated with outstanding

instructions and further it is inherent that the instruction is relative to all other

instructions in some manner. This relation could simply be instruction order, which

would then mean that the outstanding instruction is relative to the other instructions in

that some are before it and some after in program order. The examiner notes that there

is no indication of what relation exists between the instructions or to what extent.

### *Conclusion*

35.    **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

36.    The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments

avoid such references or objections.

37.    The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. The previously cited references remain pertinent and are cited

herein as well.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-

4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).
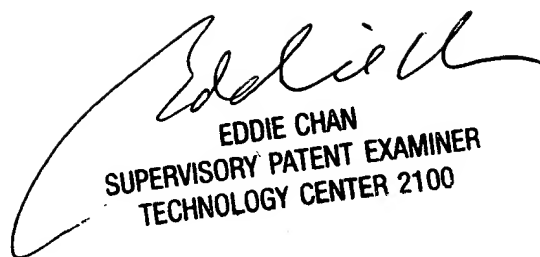
Shane F Gerstl
Examiner
Art Unit 2183

SFG
October 15, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100